REMARKS

These amendments and remarks are being filed in response to the Office Action dated November 20, 2002. For the following reasons this application should be allowed, and the case passed to issue.

No new matter is introduced by this amendment. The amendment to claim 1 is supported by originally filed claims 7 and 9. The amendment to claim 8 merely corrects claim dependency. The amendment to the specification merely corrects informalities in drawing detail numbering. Support for new claim 21 is found in the specification at page 7, line 1. Support for new claim 22 is found in the specification at page 6, lines 15-19.

Drawings

The Drawings have been objected to as failing to comply with 37 C.F.R. § 1.84(4) and 1.84(5).

In response to this objection, A Request For Approval Of Drawing Amendment has been filed in an attached separate paper. Figure 7 has been amended to show detail 58. Figures 8 and 9 have been amended to eliminate duplicate reference numbers. In addition, the specification has been amended to renumber the details referenced in Figures 8 and 9. Applicants submit that the amended Drawings comport with the requirements of 37 C.F.R. § 1.84(4) and (5).

Claim Rejections Under 35 U.S.C. § 103

Claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art (Figure 7) in view of Tuan et al. (U.S. Pat. App. 2002/0151141) and Hobbs et al. (U.S. Patent No. 6,171,910). This rejection is traversed, and reconsideration

and withdrawal thereof respectfully requested. The following is a comparison between the invention as claimed and the cited prior art.

An aspect of the invention, per claim 1, is a wafer comprising a base layer and an active layer formed on the base layer. A gate dielectric layer is formed on the active layer, a conductive layer is formed on the gate dielectric layer, and a plurality of isolation regions are formed in the wafer. The wafer is divided into a plurality of first portions, second portions, and third portions. The first portions comprise gate dielectric capacitors. The gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer. The first electrode layer is formed from the active layer. The insulating layer is formed from the gate dielectric layer and the second electrode layer is formed from the conductive layer. The second portions comprise first dummy structures. The first dummy structures comprise a first electrode layer and an insulating layer. The first electrode layer of the first dummy structures is formed from the active layer and the insulating layer of the first dummy structures is formed from the gate dielectric layer. The second portion does not contain the conductive layer. The third portions comprise second dummy structures, the second dummy structures comprise an insulating layer and a second electrode layer. The insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from the conductive layer. The third portion does not contain the active layer.

The Examiner asserted that Prior Art Figure 7 of the instant specification teaches a wafer comprising a base layer, gate dielectric layer, conductive layer, active region, a plurality of shallow isolation regions, and a metal interconnect. The Examiner acknowledged that the admitted prior art does not teach a wafer divided into a plurality of

the claimed first, second, and third portions. The Examiner relied on Tuan et al. to provide a teaching of the third portion (second dummy structure) and Hobbs et al. to provide a teachign of the second portion (first dummy structure). The Examiner averred that Tuan et al. dummy structures 141 correspond to the claimed second dummy structure and that Hobbs et al. dummy structures 201 & 202 correspond to the claimed first dummy structure. The Examiner concluded that it would have been obvious to modify the Admitted Prior Art gate structure to include the dummy structures of Tuan et al. and Hobbs et al. to reduce tunneling leakage.

The Admitted Prior art, Tuan et al., and Hobbs et al., whether taken alone, or in combination, do not suggest the claimed wafer. The Examiner proposed combination does not disclose or suggest the claimed first dummy structure. Contrary to the Examiner's assertion, Hobbs et al. do not disclose the claimed first dummy structure. The dummy structures of Hobbs et al. are merely temporary intermediary structures. Hobbs et al. (column 4, line 42 to col. 6, line 5) teach that the dummy gate electrodes are etched, and then new gate electrodes are subsequently formed from different gate electrode materials. Thus, the dummy structures of Hobbs et al. do not exist when the Hobbs et al. semiconductor device is completed.

There is **no** motivation in Hobbs et al. to substitute an intermediary product with dummy gates into the Admitted Prior Art structure.

Furthermore, the dummy gate structures of Tuan et al. protect circuit elements during chemical-mechanical polishing. The dummy structures of Hobbs et al. are intermediary structures formed during the manufacture of a different final product. There is

no motivation to combine these two very different structures, which are formed for very different reasons, with the field effect transistor (FET) of the Admitted Prior Art.

The Examiner asserted that it would have been obvious to "modify the gate dielectric structure of Admitted Prior Art Figure 7 with the first, second, and third portions of Tuan et al. and the dummy structures of Hobbs et al. to reduce tunneling leakage." The Examiner did not explain, however, where Tuan et al. or Hobbs et al. teach the alleged motivation.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion in Tuan et al. or Hobbs et al. of substituting the claimed first and second dummy structures into the wafer of the Admitted Prior Art.

The mere fact that references can be modified does not render the resulting combination obvious unless the prior art also suggests the desirability the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Tuan et al. and Hobbs et al. do not suggest the desirability of forming a wafer comprising the claimed first and second dummy structures and a FET.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific

reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation in Tuan et al. or Hobbs et al. to form a wafer comprising the claimed first and second dummy structures and a FET.

The only teaching of the claimed wafer comprising a plurality of first portions, second portions comprising a first dummy structure, and third portions comprising a second dummy structure is found in Applicants' disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner's conclusion of obviousness is not supported by any factual evidence. The Examiner has not provided a factual basis for asserting that the combination of the Admitted Prior Art, Tuan et al., and Hobbs et al. would provide the claimed invention. The Examiner's retrospective assessment of the claimed invention and use of unsupported conclusory statements are not legally sufficient to generate a case of *prima facie* obviousness. The motivation for modifying the prior art must come from the prior art and must be based on facts.

In light of the amendments and remarks above, this application is in condition for allowance, and the case should be passed to issue. If there are any questions regarding this

Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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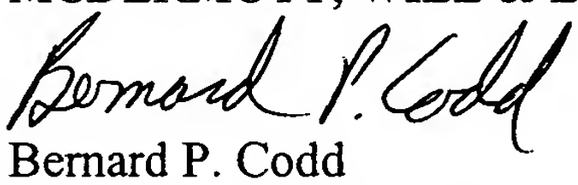

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at line 9 of page 7 has been amended as follows:

In other embodiments different gate dielectric layers are formed on a wafer comprising shallow trench isolation regions. FIG. 8 illustrates a wafer [50] 150 comprising a silicon base layer [12] 152 and a plurality of shallow trench isolation regions [54] 154. A gate oxide layer [56] 156 is formed on the silicon base layer [12] 152 by thermal oxidation of silicon layer [12] 152 or by silicon oxide deposition techniques. After the formation of the gate oxide layer [56] 156, a mask is formed over the wafer [50] 150 and selected first portions of the gate oxide layer [56] 156 are removed by etching. A first alternate dielectric is subsequently deposited where the first portions of the gate oxide layer [56] 156 were removed. Alternate dielectrics include high-k dielectrics, nitride stack dielectrics, and other known dielectrics. After depositing the first alternate dielectric, the wafer [50] 150 is again masked and second portions of the gate oxide layer [56] 156 are removed by etching. A second alternate dielectric is deposited where the second portions of the gate oxide layer were removed. Masking, etching, and alternate dielectric deposition is repeated until a desired number of different types of dielectric layers are deposited. An exemplary embodiment comprising different types of gate dielectrics is shown in FIG. 9, which comprises a high-k dielectric layer [60] 160, a nitride stack dielectric layer [58] 158, and a gate oxide layer [56] 156.

IN THE CLAIMS:

Claims 1 and 8 have been amended as follows:

1. (Amended) A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.

8. (Amended) The wafer of claim [7] 1, further comprising a silicon electrode contacting an isolation region.

Claims 7 and 9 have been canceled.

New claims 21 and 22 have been added.